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**REMARKS**

In the present Office Action, claims 1 - 12 were examined. Claims 13 - 20 are withdrawn. Claims 1 - 12 are rejected, no claims are objected to or allowed.

By this Amendment, claim 1 has been amended. No claims have been canceled or added. Accordingly, claims 1 - 12 are presented for further examination. No new matter has been added. By this Amendment, claims 1 - 12 are believed to be in condition for allowance.

**Explanation of Above Amendments**

Applicants' claim 1 has been amended to more precisely identify that there are a plurality of electrically isolated routing circuits and that these routing circuits electrically interconnect individual combinations of lands and chip attach sites. This is in accord with Applicants' specification (International Publication WO2006/0151860A1) at paragraph [0035]. The amendment more precisely distinguishes the routing circuits of Applicants' claimed invention from a single die pad electrically connected to the entire backside of an integrated circuit device.

Applicants' invention, as embodied in claim 1, is drawn to a package for encasing at least one semiconductor device. The package includes a lead frame that has a plurality of electrically isolated routing circuits extending from an array of lands for bonding to external circuitry to an array of chip attach sites that are directly electrically interconnected to input/output pads on the semiconductor device. A first molding compound is disposed between individual lands of the array of lands and a second molding compound encapsulates the semiconductor device, the array of chip attach sites and the routing circuits.

With further reference to claim 1, the expression "directly electrically interconnected" is defined in US 2006/0151860 A1 at paragraph [0036] to define the interconnection as a flip chip method without the use of an intervening wire bond or tape automated bonding tape. As shown in both references applied against claim 1, US 6,664,615 and US 6,670,222, when a wire bond is employed, the wire bond extends beyond the perimeter of the integrated circuit device increasing the footprint of the reference packages. No such wire bond is required in Applicants' package.

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employed, the wire bond extends beyond the perimeter of the integrated circuit device increasing the footprint of the reference packages. No such wire bond is required in Applicants' package.

Applicants' claim 1 was rejected under 35 USC 103(a) as unpatentable over *Bayan, et al.* (US 6,664,615) in view of *Brodsky* (US 6,670,222). The Examiner indicated that *Bayan, et al.* teach a package having a lead frame with a first end 750 terminating at an array of lands adapted to be bonded to external circuitry 790 and a second end directly interconnected to an input/output pad 710 on at least one semiconductor device. Applicants respectfully note that the structure 710 is defined in US 6,664,615 at column 5, lines 44-48 as a die attach material. While such a die attach material may be electrically insulating or electrically conductive, Applicants have not located a recitation of electrical conductivity in the disclosure of the die attach material in US 6,664,615. Applicants note that the I/O pads (referred to in US 6,664,615 as die terminals) are identified by reference numeral 670 and are connected to the lead frame by wire bond 680. There is nothing in US 6,664,615 to teach or suggest I/O pads, die terminals, that are directly attached to a lead frame.

US 6,670,222 discloses a package substrate 91 that may include a metallized layer 97 having a plurality of indentations formed therethrough. The metallized layer is joined to the backside of the semiconductor device 92 by a die attach adhesive that may be electrically conductive. However, the only electrical interconnections to I/O pads on the semiconductor device are by way of wire bonds 102. The die attach adhesive merely provides a common, *i.e.* not electrically isolated, voltage source to the backside of the semiconductor device.

Neither US 6,664,615 nor US 6,670,222 teaches or suggests a plurality of electrically isolated routing circuits, electrically interconnecting individual combinations of lands and chip attach sites where the chip attach sites are directly electrically interconnected (*i.e.* without wire bonding) to input/out pads on at least one semiconductor device. There is nothing in the combination of references to teach or suggest the claimed structure. Applicants' claim 1 should be allowed over the combination of references. Dependent claims 2-12 further limit and define claim 1 and should likewise be in condition for allowance.

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Applicants' amendment is intended to place the claims in condition for allowance, or in the alternative in better condition for appeal, and is not believed to add subject matter to the claims requiring further search and as such is proper under the requirements of 37 CFR 1.116. Entry of this amendment and reconsideration of the claims as amended is respectfully requested.

### **NOTICE OF APPEAL**

Applicants enclose a notice of appeal in the event that rejection of the pending claims is maintained.

### **PETITION FOR AN EXTENSION OF TIME**

A petition under 37 CFR 1.136(a) requesting a one month extension in the period to respond to the outstanding office action is enclosed.

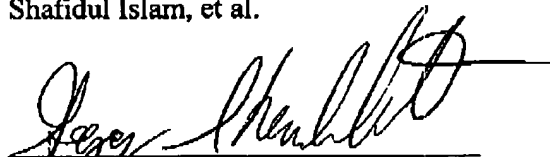
Accordingly, Applicants submit that none of the references, alone or in combination, anticipate or make obvious the invention as presently claimed and that the application is now in condition for allowance. Therefore, Applicants respectfully request reconsideration and further examination of the application and the Examiner is respectfully requested to take such proper actions so that a patent will issue herefrom as soon as possible.

If the Examiner has any questions or believes that a discussion with Applicant's attorney would expedite prosecution, the Examiner is invited and encouraged to contact the undersigned at the telephone number below.

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Respectfully submitted,  
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Date: April 22, 2008

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